C\_OW\_CTRL

Revision History

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# C\_OW\_CTRL

## Introduction

C\_OW\_CTRL generates current control signals CS\_EN\_AUTO\_SINK and CS\_EN\_AUTO\_SOURCE, outputs twice ADC single conversion start(C\_OW\_ADC\_GO) and monitors whether ADC measurement results exceed the specified voltage range.

### Main features

The C\_OW\_CTRL module has the following features:

• Programmable current time up to 32ms by 2ms per step

• Independent over range flag for each CELL

## Functional Details

### Block Diagram

C\_OW\_CTRL block diagram shows in Fig1.



Fig C\_OW\_CTRL control flow Diagram

C\_OW\_CTRL I/O signals description shows in table.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pin Name | Direction | Width | Default Value | Duration | Description |
| resetb\_SR\_CLK | Input | 1b' | 1'b1 | N/A | Asynchronous power on reset, release synchronously in CLK\_32M domain. |
| rstb\_32M\_ok\_and\_sr | Input | 1b' | 1'b1 | N/A | soft reset, CLK\_32M\_OK low reset |
| SOFT\_RSTB\_REG | Input | 1b' | 1'b1 | N/A | soft reset; release synchronously in CLK\_32M domain. |
| CLK\_REG\_SC | Input | 1b' | 1'b0 | 125ns | 8MHZ |
| CLK\_32M\_OK | Input | 1b' | 1'b0 | N/A | CLK\_32M\_OK |
| C\_OW\_DET\_GO | Input | 1b' | 1'b0 | N/A | C\_OW\_CTRL star |
| clr\_ADC\_GO | Input | 1b' | 1'b0 | 8us | ADC\_GO clear |
| RR\_END | Input | 1b' | 1'b0 | 8us | Round-robin end flag |
| C\_OW\_TDIS\_REG | Input | 4b' | 4'h0 | N/A | C\_OW\_TDIS\_REG shall cover from 2ms to 32ms  4’h0: 2ms  4’h1: 4ms  4’h2: 8ms  …  4’h15: 32ms |
| CELL\_ADC\_DATA\_CH1  -CELL\_ADC\_DATA\_CH18 | Input | 16b' | 16'h8000 | N/A | ADC converted data of CELL1-CELL18 without DLPF |
| C\_OW\_FLT | Output | 19b' | 19'h0 | N/A | Over range flags |
| clr\_C\_OW\_DET\_GO | Output | 1b' | 1'b0 | 1 CLK\_REG | C\_OW\_DET\_GO clear signal |
| CS\_EN\_AUTO\_SINK | Output | 1b' | 1'b0 | 3\*TDIS |  |
| CS\_EN\_AUTO\_SOURCE | Output | 1b' | 1'b0 | 1\*TDIS |  |
| C\_OW\_ADC\_GO | Output | 1b' | 1'b0 |  | ADC single conversion go, it is cleared by clr\_ADC\_GO |

### Control flow

C\_OW\_CTRL work control flow shows in Fig2. C\_OW\_CTR only loads C\_OW\_TDIS\_REG to C\_OW\_TDIS when C\_OW\_DET\_GO is high and keep the value. Besides, CS\_EN\_AUTO\_SINK　is set to 1 when C\_OW\_DET\_GO is detected high. After 3\*(C\_OW\_TDIS+1)\*2ms time delay, C\_OW\_ADC\_GO is set to 1 the first time to start Cn open wire detection. C\_OW\_ADC\_GO is cleared to 0 by clr\_ADC\_GO generated by ADC\_CTRL. Until a single round-robin conversion is finished(RR\_END from ADC\_CTRL is asserted), CS\_EN\_AUTO\_SINK can be cleared to 0 and CS\_EN\_AUTO\_SOURCE will be asserted. When the first RR\_END is high, it compares measurement result of CELL1 with 0.1V, the other CELL results compare with -0.4V, any CELL measurement result over range will be recorded to C\_OW[18:1], After a delay of C\_OW\_TDIS\*2ms time, C\_OW\_ADC\_GO is set to 1 the second time. Until a single round-robin conversion is finished(RR\_END from ADC\_CTRL is asserted), CS\_EN\_AUTO\_SOURCE can be cleared to 0. When the second RR\_END is high, it only compares measurement result of CELL1 with -0.4V, if the measurement over range C\_OW[0] will be asserted high.



Fig C\_OW\_CTRL control flow Diagram

### State Machine

C\_OW\_CTRL is mainly implemented by a state machine shows in Fig3.

As shown in Fig3, C\_OW\_AUTO1\_STAT controls to generate CS\_EN\_AUTO\_SINK and the first C\_OW\_ADC\_GO, C\_OW\_AUTO2\_STAT controls to generate CS\_EN\_AUTO\_SOURCE and the second C\_OW\_ADC\_GO. The c\_ow\_cnt is the delay counter, which is automatically incremented by one when another counter(counter\_2ms) reaches 14’d16000. The c\_ow\_cnt is cleared to 0 when RR\_END is high or CLK\_32M\_OK is low.

C\_OW\_CTRL state machine will be reset when CLK\_32M\_OK is low. The state machine switches to C\_OW\_AUTO1\_STAT state from IDLE state when C\_OW\_DET\_GO is high, and exit from C\_OW\_AUTO1\_STAT state to C\_OW\_AUTO2\_STAT state by swap1 is valid(c\_ow\_cnt more than 3\*C\_OW\_TDIS and RR\_END is high), then return to IDLE state by swap2 is valid(c\_ow\_cnt more than C\_OW\_TDIS and RR\_END is high). When the state machine enters the C\_OW\_AUTO1\_STAT state, a clr\_C\_OW\_DET\_GO signal is generated to clear clr\_C\_OW\_DET\_GO to 0.



Fig C\_OW\_CTRL state machine flow

If ADC is busy, in order to obtain correct Cn open wire measurement results, it is advised to disable ADC before write 1 to the DLAG\_CTRL1[C\_OW\_DET\_GO] bit.